IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: B. Davis et al.

Filed: December 28, 2000

Title: NUMA SYSTEM RESOURCE DESCRIPTORS INCLUDING PERFORMANCE CHARACTERISTICS

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Before calculation of the filing fee or examination, please amend the above-identified application as follows:

In the Specification

On page 8, at line 29: change "node" to —processor—, and change "64" to —140—.

In the Claims

Please amend the claims to read in full as follows:

1. (Amended) A computer system, comprising:

multiple processors,

a plurality of resources assigned to node groups;

a first descriptor of respective topological levels of at least one of the resources; and

a second descriptor of respective performance of said resources ,

wherein the first and second descriptors are produced by firmware .

2. (Unchanged) The system of claim 1, wherein said first descriptor is a first level data structure, and said second descriptor is a primary data structure.

3. (Unchanged) The system of claim 1, wherein said primary data structure comprises a pointer to a secondary data structure.

4. (Unchanged) The system of claim 1, further comprising a node identifier for each node for identifying positional placement of a resource.

5. (Unchanged) The system of claim 4, wherein said node identifier represents multiple levels of interconnect.

6. (Unchanged) The system of claim 1, further comprising a dynamic updator of at least the first and second descriptors.

7. (Unchanged) The system of claim 6, wherein said dynamic updator reflects real-time system configuration into the first descriptor.

8. (Unchanged) The system of claim 6, wherein said dynamic updator reflects real-time system performance into the second descriptor.

9. (Unchanged) The system of claim 1, wherein said second descriptor is selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors and shared cache descriptors.

10. (Amended) The system of claim 9, wherein said shared cache descriptor reflects [interconnect] interconnects of the system.

11. (Unchanged) The system of claim 10, wherein said shared cache descriptor reflects latencies of the interconnects.

12. (Unchanged) The system of claim 1, wherein said first descriptor reflects average latency between the node groups.

13. (Amended) An article comprising:

a computer-readable signal bearing medium readable by a computer having multiple processors and a plurality of resources assigned to node groups;

means in the medium for determining topological levels of at least some of the resources; and

means in the medium for determining performance of said resources ,

wherein said topological level determining means and said performance determining means are capable of being stored in firmware of the system.

14. (Unchanged) The article of claim 13, wherein the medium is a recordable data storage medium.

15. (Unchanged) The article of claim 13, wherein the medium is a modulated carrier signal.

16. (Unchanged) The article of claim 13, wherein said topological level determining means is a first descriptor and said performance determining means is a second descriptor.

17. (Unchanged) The article of claim 13, further comprising a node identifier for identifying positional placement of a resource for each node.

18. (Unchanged) The article of claim 16, wherein said second descriptor is selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors and shared cache descriptors.

19. (Unchanged) The article of claim 13, wherein said second descriptor comprises a shared cache descriptor which reflects interconnect of resources.

20. (Unchanged) The article of claim 19, wherein said shared cache descriptor reflects latencies of the interconnects.

21. (Unchanged) The system of claim 16, wherein said second descriptor reflects average latencies between node groups.

22. (Amended) A method for enabling allocation of resources in a multiprocessor, comprising:

assigning multiple resources into node groups; and

maintaining system resource topology and performance descriptions as at least one data structure produced by firmware .

23. (Unchanged) The method of claim 22, further comprising

traversing the data structure to enable allocation of at least some of the resources.

24. (Unchanged) The method of claim 22, wherein said traversal step includes accessing a second data structure.

25. (Unchanged) The method of claim 24, wherein said secondary data structure is selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors and shared cache descriptors.

26. (Unchanged) The method of claim 24, wherein said secondary data structure includes a shared cache descriptor for describing at least part of a system interconnect including latency between sibling nodes.

27. (Unchanged) The method of claim 22, further comprising maintaining at least average latency between at least two of the nodes.

28. (Unchanged) The method of claim 22, wherein said traversal step includes recursively accessing additional data structure levels.

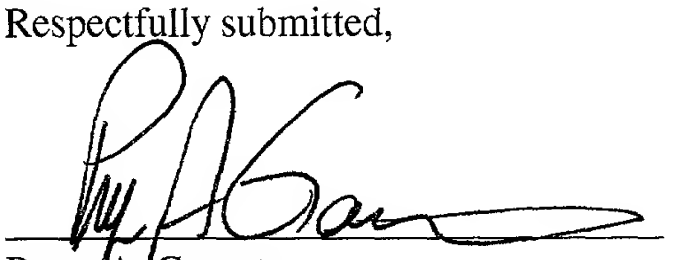
REMARKS

By this amendment Applicants have corrected a typographical error on page 8 of the Specification, and have amended the claims to more particularly point out the patentable aspects of their invention. No new matter has been added by these amendments.

Applicants respectfully request early and favorable consideration of this application and allowance of all claims presented.

The Examiner is urged to call the undersigned at the below-listed telephone number if, in the Examiner's opinion, such a phone conference would expedite or aid in the prosecution of this application.

Respectfully submitted,



Pryor A. Garnett
Attorney for Applicants
Registration No. 32,136

IBM Corporation
IP Law Dept., EDO2-805
15450 SW Koll Parkway
Beaverton, OR 97006-6063

Telephone: (503) 578-5020
Fax: (503) 578-5040